Amendment to the claims:

1-10.   (Canceled).

11.   (Currently Amended) An information processing unit,
~~adding instruction codes which are different from each other in the same group of~~
~~instruction to each instruction, and sorting the instructions executable into a plurality of groups~~
~~of instructions,~~
comprising a decoder circuit selecting <u>an instruction</u> ~~the~~ group ~~of instruction~~
corresponding to ~~the~~ <u>an inputted</u> instruction code ~~inputted thereto~~, based on <u>a</u> ~~input~~ history of
the <u>inputted</u> instruction code, <u>and uniquely</u> ~~to determine the~~ <u>an</u> instruction to be executed
<u>selected from a plurality of executable instructions in accordance with the inputted</u> ~~uniquely by~~
~~the~~ instruction code ~~inputted thereto~~, and
~~setting a prescribed instruction code, which assigns an optional instruction depending~~
~~on the other group of instruction, to each group of instructions, and wherein said decoder circuit~~
~~controls to execute the instruction which is assigned to said prescribed instruction code, when~~
~~said prescribed instruction code is inputted~~
<u>wherein said plurality of executable instructions are sorted into a plurality of instruction</u>
<u>groups and each instruction is given with an instruction code different from others within the</u>
<u>same instruction group in advance, each instruction group having a certain instruction code to</u>
<u>which an instruction belonging to another instruction group can be assigned, and said decoder</u>
<u>circuit outputting a control signal corresponding to the instruction assigned to the certain</u>
<u>instruction code to a processor element, when said certain instruction code is inputted</u>.

12.   (Currently Amended) The information processing unit according to claim 11,
wherein ~~said~~ <u>the</u> instruction<u>, which belongs to another</u> ~~depending on the other group of~~
instruction<u>,</u> ~~which~~ <u>group and</u> is assigned to ~~said prescribed~~ <u>the certain</u> instruction code, ~~can be~~
<u>is changeable</u> ~~changed~~.

13.   (Currently Amended) The information processing unit according to claim 11,
wherein ~~a plurality of said prescribed~~ <u>each of the</u> instruction <u>groups has a plurality of the certain</u>
instruction codes[[,]] <u>to</u> which <u>an instruction belonging to the other instruction</u> ~~assign optional~~

2

instructions depending on the other group can be assigned. of instruction, are provided to groups of the instruction.

14.   (Currently Amended) An information processing unit,

adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions, and

comprising a decoder circuit holding a prescribed information corresponding to input history of the instruction codes, selecting the group of the instruction corresponding to the instruction code inputted thereto, based on said prescribed information, to determine the instruction to be executed uniquely by the instruction code inputted thereto, retaining information corresponding to a history of inputted instruction codes, selecting an instruction group corresponding to an inputted instruction code based on the information, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code, and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups and each instruction is given with an decoder circuit changes said prescribed information temporary, when a prescribed instruction code different from other instruction codes within the same instruction group in advance, and said decoder circuit temporarily changes the information when a certain instruction code is inputted.

15.   (Currently Amended) The information processing unit according to claim 14, wherein said decoder circuit determines [[the]] an instruction to be executed, regardless of said prescribed based on the inputted instruction code only, irrespective of the information corresponding to the input history of [[the]] instruction codes, when an instruction code for determining the , in which an instruction to be executed uniquely by only in accordance with the instruction code only is uniquely determined, is inputted thereto is inputted.

16.   (Currently Amended) An information processing unit executing an instruction which is determined by an in accordance with an inputted instruction code inputted thereto,

comprising a decoder circuit holding a prescribed retaining information corresponding to an input history of a plurality of inputted instruction codes inputted thereto, and uniquely

determining [[the]] an instruction to be executed ~~uniquely, based on the instruction code~~ ~~inputted thereto as well as the prescribed information,~~ selected from a plurality of instructions which are assigned to the [[said]] inputted instruction code ~~inputted thereto~~ in accordance with a combination of the information and the inputted instruction code.

17. (Currently Amended) The information processing unit according to claim 16, wherein the ~~instructions executable are sorted into a plurality of groups of instructions and the~~ ~~instruction codes which are different from each other in the same group are added to each~~ ~~instruction~~ decoder circuit determines an instruction to be executed selected from a plurality of executable instructions, and the plurality of executable instructions are sorted into a plurality of instruction groups and each instruction is given with an instruction code different from others within the same instruction group in advance.

18. (Currently Amended) The information processing unit according to claim 16, wherein said decoder circuit determines [[the]] an instruction to be executed, ~~regardless of said~~ ~~prescribed~~ based on the inputted instruction code only, irrespective of the information corresponding to the ~~input history of the~~ history of instruction codes, when an instruction code ~~for determining the instruction to be executed uniquely by only the instruction code inputted~~ ~~thereto is inputted~~ , in which an instruction to be executed in accordance with the instruction code only is uniquely determined, is inputted.

19. (Currently Amended) An information processing unit, comprising a plurality of processors on one chip, each processor capable of executing ~~which execute~~ instructions independently ~~in one chip, wherein the instructions executable by said processor are sorted into a~~ ~~plurality of groups of instructions indicated by a group code, with the instruction codes which are~~ ~~different from each other in the same group of instruction being added to each instruction, and~~ ~~wherein said each processor comprises a decoder circuit which determines the~~ , wherein each of said processors comprises:
    a decoder circuit uniquely determining an instruction to be executed ~~uniquely~~ selected from a plurality of executable instructions based on [[said]] an inputted instruction code and a group code corresponding to ~~input~~ a history of the inputted instruction codes ~~and the instruction code inputted~~ ~~thereto~~, and

a processor element ~~which executes~~ executing an operation corresponding to a control signal ~~supplied~~ provided from said decoder circuit, and ~~wherein the instruction executable by said processor~~

wherein said plurality of executable instructions are sorted into a plurality of instruction groups assigned by the group code and each instruction is given with an instruction code different from others within the same instruction group in advance, and the executable instruction includes an alias instruction ~~which assigns in advance the optional instruction for the~~ to which an instruction belonging to the other instruction group can be assigned in advance to an internal instruction code ~~generated~~ constituted by the group code and the inputted instruction code.

20.   (Currently Amended) The information processing unit according to claim 19, wherein ~~said~~ each ~~processor~~ of said processors further comprises a group ~~resister which stores~~ register storing the group ~~codes set on the basis of the input~~ code, which is set up based on the history of ~~said~~ the inputted instruction code.

21.   (Currently Amended) The information processing unit according to claim 20, wherein ~~said~~ each ~~processors~~ of said processors further comprises a ~~look up~~ lookup table ~~which defines the rule for changing~~ prescribing a change in a rule of the group code stored in said group register.

22.   (Currently Amended) The information processing unit according to claim 21, wherein said ~~look up~~ lookup table ~~defines~~ is set up with a combination of an instruction mask for setting a mask bit ~~to be masked~~, an instruction code for comparing the ~~instruction with the~~ internal instruction code ~~generated by the group code and the input instruction code~~, and [[a]] the changed group code.

23.   (New) The information processing unit according to claim 11, wherein each instruction group is given with a group code different from others in the instruction group in advance, and the group code corresponding to the inputted instruction code is determined based on the history of the inputted instruction code.

24.   (New) The information processing unit according to claim 14, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.

25.   (New) The information processing unit according to claim 17, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.